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Bluetooth Single Chip Radios: Holy Grail or White Elephant?

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Achieving a $5 Bluetooth Implementation

The emerging Bluetooth market is highly cost sensitive and chip manufacturers are striving to produce the lowest priced components possible. The stated goal is to implement Bluetooth for less than five dollars. Radio designers have proclaimed for years that the ultimate way to achieve the lowest cost and smallest footprint is to develop a single chip radio. With the Bluetooth standard and processes such as CMOS, the single chip Holy Grail seems well within reach.

On the surface, it would appear that the single chip would be the obvious choice providing the smallest and lowest cost approach. But a careful examination reveals more to the story. There is more to implementing Bluetooth than the price of the chip, including antenna design and placement, software and its associated memory requirements, and external biasing and matching components. And not all Bluetooth applications are equal. There is a wide range of potential markets such as cell phones, laptop computers, PDAs, headphones, keyboards, and digital cameras, and it is difficult to come up with one design that can address all these markets and still maintain a small chip size.

Optimizing Designs for Lowest BOM Cost

By taking a “tops down” approach, one can design a solution that is optimized to produce the lowest bill of materials (BOM). This paper will examine the two most common approaches: a single chip solution containing both the high frequency transceiver and the baseband functions combined on one IC, and a two chip approach in which the baseband controller functions and the radio functions are implemented separately.

Reducing Test Costs

One of the biggest challenges in Bluetooth design is production test. On the transceiver side, Bluetooth ICs have a 2.4GHz high frequency interface requiring analog test metrics such as power, noise figure, adjacent channel interference and intermodulation. Opposite that is a purely digital interface that is tested using vector scan test methodologies.

Digital testers are abundantly available from companies such as Teradyne who produces the Integra J750 tester for as low $70k per site. To achieve test efficiency, several components can be tested in parallel reducing test time by electrically evaluating several components simultaneously and by minimizing the indexing time – the time it takes to remove and replace one set of components being tested. Saving on index time can be significant since it can be as high as 35% of total test time for single unit tests. For a design with the level of complexity of Bluetooth, one can expect to be able to test four units in parallel with an overall throughput of 4600 units per hour including indexing time, resulting in test cost of around $ 0.02 per device.

On the other hand, Mixed signal testers with RF capability, such as Teradyne’s Catalyst SoC tester, are much more complicated to manufacture and typically cost around $1.2M depending on the options selected. While RF multi-site testing can be performed, it is usually limited to four devices in parallel and requires careful shielding. For multi-site testing on a mixed signal tester, the cost is typically $300k per site, significantly higher than for digital testing. The highest throughput that can be achieved is approximately 2750 units per hour, assuming a four site test and a test time below 4.5 sec., resulting in test cost of around $ 0.08 per device.

Test costs are directly proportional to the capital cost of equipment divided by the overall throughput. If the radio and controller sections are implemented separately, the baseband controller IC can be tested very inexpensively. The radio IC, which requires the high frequency measurement capability, must be tested on the more expensive equipment. If the two functions are combined on the same chip, then both functions must be tested on the more expensive mixed signal tester, thus driving up the test cost of the digital baseband portion.

Optimizing Test Yield

Yield further complicates the problem. The digital baseband controller section will typically yield much higher than the RF section of the chip. Minor process variations have little effect on a digital gate’s ability to switch states, but may have significant affect on gain, noise or linearity of the analog section. If the two sections are tested separately, a digital baseband controller would typically yield as high as 98% whereas the radio portion may only yield 80-90%. Even companies using on-chip calibration in their single chip design are reporting RF yields below 90%. If these two functions are combined into a single chip and the radio portion is not within acceptable limits, then even if the baseband controller is working perfectly, it must be discarded along with the radio, driving the baseband controller yield down to match that of the analog radio. This will significantly increase the cost of the overall solution.

Maximum Market Flexibility

The Bluetooth specification defines the characteristics of RF energy being emitted by the antenna. A companion specification, the BlueRF interface, defines how data is to be passed from the radio IC to the baseband controller. Because the radio is highly constrained by specifications, the main differentiators will be size, power consumption and cost. The baseband, on the other hand, must interface with numerous products from cell phones to computers, PDAs, digital cameras, mouse and keyboards, headphones, Internet access points, and applications limited only by one’s imagination. This plethora of interfaces can be addressed by providing specialized baseband components optimized for specific applications. By having the radio remain a separate chip, it can be produced in very high volume, driving the cost down. The baseband chip can tailor functionality to minimize the cost for the particular application.

Moving Toward an Embedded or Software Controller

To really drive the cost down, many OEMs want to embed Bluetooth functionality onto a processor "super chip" and have the radio portion as a separate IC. The advantage of this approach is that the Bluetooth functions can make use of existing memory and processor power, allowing the Bluetooth specific functions to be added with as low as 50K gates. The radio remains separate because trying to integrate a 2.4GHz component onto a processor chip would be impractical. The connection would be through a standard BlueRF interface giving the most flexibility. With this approach, the goal of adding Bluetooth for below $5 can be achieved. One can achieve further cost reductions in the future by implementing the baseband controller in software and still using the external radio IC with its BlueRF interface. A single chip radio would not be useful in these types of applications.

Process Scaling

Another advantage to separating the radio and the baseband controller is process scaling. According to Moore's law, the area required for performing a digital function shrinks by 50% every 18 months. To take advantage of this, one would want to re-spin the IC to a smaller geometry process. For example, if one scales a design from 0.25um CMOS to 0.18um CMOS, one would expect the area to be reduced to about 30-40% of the original area for the same functionality. For a purely digital design, such as the baseband controller, this expectation is realized assuming the design is not pad limited. For the RF portion of the design, however, one would not see the same return for his or her efforts. Radio design area is dominated by passive components such as capacitors, inductors and resistors that are not affected by process scaling.

Furthermore, one must redesign the analog radio portion of the IC, the trickiest part of the design, every time the IC scales downward. Some analog circuitry, such as Gilbert Cell mixers, cannot be implemented as process technology scales downward because of the lower voltage headroom, forcing designers to select different topologies. One must also redesign input and output matching impedances, and redesign high-frequency blocks such as the Low Noise Amplifier (LNA) or the Power Amplifier (PA). Not only does this increase development time, but it can introduce significant uncertainty in the design process, often requiring additional turns of the IC design to produce working components. This can significantly increase development time for a single chip design, delaying introduction of new products to the market.

By separating the RF from the digital function, you can continue to manufacture the RF chip, driving cost down through volume, and can scale the baseband chip relatively easily to lower cost by reducing area.

Power Consumption

One might expect that a two chip approach would increase the overall power consumption, but the additional circuitry required to implement a BlueRF interface on both the baseband controller and the radio only add less than 50uA, an insignificant amount of current, making both the single chip and the two chip approach virtually identical.

Architecture Selection: Differential vs. Single Ended

Another significant difference is due to substrate noise in a CMOS process. With the presence of a baseband controller, and all its associated clock frequencies, on the same chip as a high-frequency 2.4GHz radio transceiver, the substrate noise can be greatly increased. The effects of this can be reduced by careful layout and addition of guard rings, but noise is still a significant factor. To further reduce the effects of substrate noise, designers use differential inputs to the LNA and differential outputs from the PA. The problem with this approach is that external baluns are required to provide matching to the antenna, and they add to the overall BOM cost. By moving the radio into a separate IC away from the noisy controller, the problem is greatly reduced allowing the selection of single-ended design topologies that can have all the matching circuitry on-chip and still easily pass the Bluetooth requirement for –70dBm sensitivity. One could also reduce substrate noise by selecting a process such as SiGe or SOI, but this approach would also increase cost since these processes are typically more expensive than standard CMOS.

Minimizing Circuit Board Area

The embedded controller approach also has the advantage of having the smallest footprint. A Bluetooth transceiver can be implemented in a small, 5mm x 5mm package, much smaller than a single chip radio. Thus, by separating the two functions, the smallest footprint is achieved.

Conclusion

Although single chip radios are exciting technical marvels, they do not necessarily provide the lowest overall cost. By separating the radio transceiver from the baseband controller, the greatest market flexibility is realized, manufacturing costs are reduced, the overall BOM cost is optimized, and the smallest footprint is achieved.

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